

Frequency Synthesis for 60 GHz OFDM Systems

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Abstract—This paper presents a frequency plan for a super-heterodyne OFDM transceiver for the 60 GHz band. We derive an approximation for the rms phase error of the phase-locked loop (PLL). The phase error is related to the phase noise levels of the voltage-controlled oscillator (VCO) and the crystal reference, the PLL division factor, the second-order loop parameters, and the OFDM carrier spacing. We verify our approach by comparison with the simulated phase error and BER including correction of the common phase error for a 16-QAM OFDM system. The model drastically simplifies noise optimization of PLLs.

I. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) has become popular in WLAN systems for its flexibility to adapt transmission rates, its high spectral efficiency and its robustness against multi-path fading. The unlicensed band from 57 GHz to 64 GHz provides the possibility of gigabit-per-second wireless communications. The high oxygen absorption allows aggressive frequency re-use. Furthermore, due to the short wavelength, on-chip antennas become feasible. As far as frequency synthesis is concerned, the high phase noise of 60 GHz oscillators represents the main obstacle for OFDM. For a low-cost implementation, silicon-based designs are highly desirable. The phase noise of the integrated voltage-controlled oscillators (VCO) is relatively high due to the lack of high-quality passives. As a result, the phase noise may limit the transceiver performance. This is especially critical for the 60 GHz band, since the VCO phase noise at a given frequency offset increases with the oscillation frequency. In order to generate stable radio frequencies, phase locking to a clean reference is required. This also reduces the oscillator phase noise within the bandwidth of the phase-locked loop (PLL). A first integrated PLL for 60 GHz in a SiGe BiCMOS technology was

presented recently [1].

The phase error (jitter) of a PLL is strongly correlated with the bit error rate in an OFDM system and must be minimized. This includes the minimization of the VCO phase noise mainly by improving the quality factor of the resonance circuit, but also the optimization of the loop dynamics. During the last few years, many papers on PLL jitter simulation were published [2]-[7]. They are mostly focussed on behavioral circuit simulation. For system simulations a more abstract PLL model is required to minimize the simulation time and the required knowledge on circuit level. In [8]-[10] phase noise has been discussed in the context of OFDM. The phase noise model used in these papers is based on a Wiener process, which is low-pass filtered in the PLL. In reality, a combination of high-pass filtering and low-pass filtering takes place in a PLL. This must be reflected by the PLL model.

The rms phase error can be represented as an integral of the phase noise spectrum over frequency. Due to the final length T_u of an OFDM symbol, noise frequencies much below $1/T_u$ will hardly affect the OFDM system, if the common phase error (CPE) is removed using pilot tones. As a result, a high-pass weighting function for the PLL spectrum can be used to describe the CPE correction [11]. This weighting function reduces the effect of phase noise in an OFDM system, especially, if $1/T_u$ is larger than the loop bandwidth [12]. Integrating the weighted PLL spectrum, an effective phase error σ_ϕ is obtained, which includes CPE correction.

This paper relates the effective PLL phase error σ_ϕ to circuit parameters and the OFDM symbol length. A strong correlation of σ_ϕ with the bit error rate (BER) of the OFDM system is demonstrated. The PLL phase noise performance can be optimized with little effort by minimizing σ_ϕ .

II. FREQUENCY PLAN FOR OFDM TRANSCEIVER

The existing IEEE 802.11a standard is perfectly suited for data transmission at moderate data rates under difficult channel conditions. A combination of such a system with a high-rate OFDM system at 60 GHz in a silicon-based low-cost implementation would be perfectly suited for a wide range of applications. Using an intermediate frequency (IF) of 5 GHz for our 60 GHz system allows re-use of circuit blocks developed for IEEE 802.11a.

The design of a programmable PLL at 60 GHz turns out to be difficult. We favor a super-heterodyne architecture with a programmable PLL around 5 GHz for three reasons. First, compatibility to the IEEE 802.11a WLAN standard is facilitated. Second, tuning over 1-2 GHz seems possible with an integrated solution in this frequency range. Third, the image frequency is about 10 GHz away from the channel and can be filtered out by an integrated narrowband low-noise amplifier.

The first down-conversion of the potential OFDM band from 57 to 64 GHz can be performed by using a fixed-frequency PLL at 56 GHz as illustrated in Fig. 1. Here we have subdivided the whole spec-

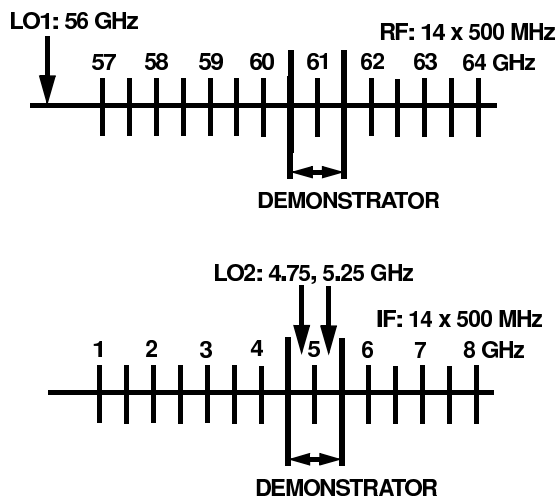


Fig. 1. Potential OFDM band and its subdivision into 14 subbands of 500 MHz before and after first down-conversion. Thick lines indicate band of a first demonstrator.

trum into subbands of 500 MHz. Focusing on the frequency range around 61 GHz, we need a PLL around 5 GHz for the second down-conversion to baseband also shown in Fig. 1. In order to relax the filter requirements, only 400 MHz of a 500 MHz band will be used, while the remaining 100 MHz serve as guard bands as shown in Fig. 2.

A possible realization of a fixed-frequency RF synthesizer as presented in [1] is shown in Fig. 3.

BB: 500 MHz total = 400 MHz useful + 100 MHz guard

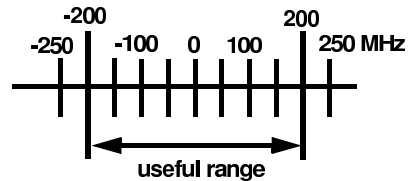


Fig. 2. OFDM subband after second down-conversion. Thick lines indicate useful range.

It generates a signal of 56 GHz for the first down-conversion. The IF PLL shown in Fig. 4 selects

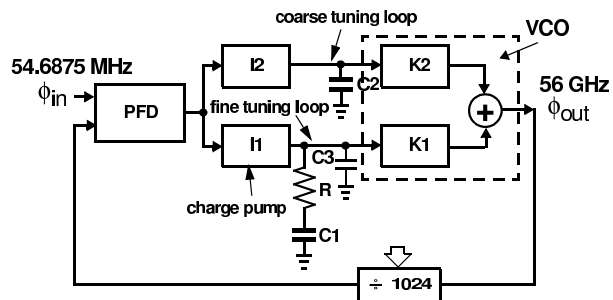


Fig. 3. Possible realization of a 56 GHz PLL for the first down-conversion.

between the two subbands ranging from 60.5-61 GHz and 61-61.5 GHz, respectively. However, it can theoretically be extended to all 14 subbands, provided that the VCO has enough tuning range. In order to achieve a wide tuning range at low noise, a dual-loop architecture as described in [13] is suggested. An array of switchable IF VCOs might be an option for a very wide tuning range.

The default settings of the program and swallow counter values are $P=26$ and $S=2$ resulting in an output frequency of 5.25 GHz. Together with the 56 GHz RF synthesizer, this frequency is suited for down-conversion of the 61 GHz - 61.5 GHz ISM band to baseband. In order to achieve compatibility with 802.11a, a 20 MHz frequency spacing at the PLL output is required, which corresponds to a 4 MHz input frequency. Both the 4 MHz for 802.11a and the 5 MHz required for the suggested 60 GHz implementation can be derived from the same crystal oscillating at $M \times (20 \text{ MHz})$ by dividing the frequency by 5M or 4M, respectively, where M is an integer number.

III. PHASE NOISE MODEL

Figure 5 shows a schematic view of an integer-N charge-pump PLL as used in modern communication

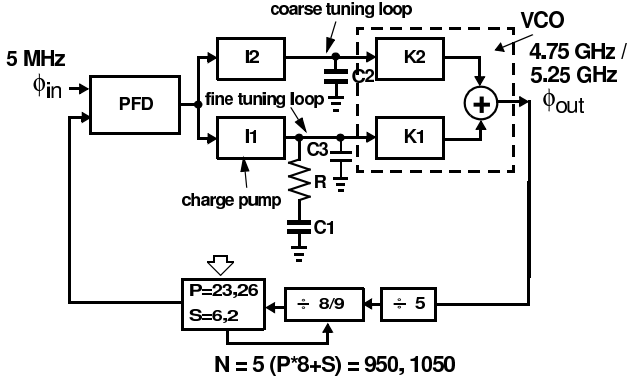


Fig. 4. Possible realization of a programmable IF PLL for the second down-conversion.

systems. A PLL locks a noisy VCO to a relatively clean reference oscillator, typically a crystal. Since the VCO frequency is usually much higher than the reference frequency, the VCO output is divided by an integer N before the phase is compared with the reference in a phase-frequency detector (PFD). The PFD in conjunction with a charge pump (CP) charges or discharges a low-pass filter (LPF) by a current proportional to the phase error. The output of the LPF is connected to the control input of the VCO.

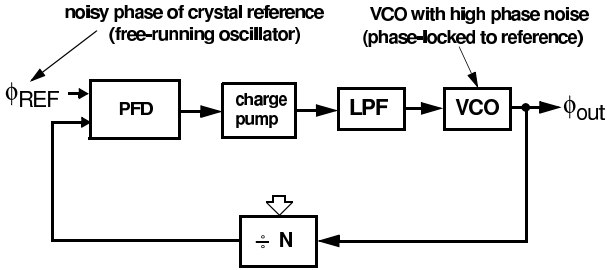


Fig. 5. Schematic view of a charge-pump PLL. The noisy VCO output is divided by N and phase-locked to a relatively clean reference to define the output frequency and to clean the VCO phase noise spectrum.

The phase noise of the free-running reference oscillator as a function of the frequency offset f can be modeled by

$$S_{REF}(f) = S_{REF}(\Delta f) \frac{(\Delta f)^2}{f^2}, \quad (1)$$

where S_{REF} is the phase noise measured at the specific offset Δf . Similarly, the phase noise of the free-running VCO is modeled by

$$S_{VCO}(f) = S_{VCO}(\Delta f) \frac{(\Delta f)^2}{f^2}. \quad (2)$$

The phase noise S can be determined from the single-sideband phase noise \mathcal{L} in units of dBc/Hz, which

is specified in data sheets, according to

$$S = 10^{\mathcal{L}/10}. \quad (3)$$

It is important to note that \mathcal{L} must be taken at a specific offset Δf in the region of the spectrum with a -20 dB / decade slope. For moderate and large frequency offsets the single-sideband phase noise equals the power spectral density of the phase [7]. The difference between the two quantities at low offsets due to flicker noise is not relevant here, since the spectrum is high-pass filtered as explained below. The filter bandwidth for the systems we have in mind is much larger than typical flicker noise corner frequencies. Therefore, we will not distinguish between the single-sideband phase noise and the power spectral density of the phase in the remainder. As shown in [14], the reference noise in a PLL is low-pass filtered, while the noise of the VCO is high-pass filtered. The complex low-pass filter function is denoted as $H_{LPF}(s)$, where $s = j\omega = j2\pi f$. The phase noise spectrum of the reference needs to be multiplied by $N^2 |H_{LPF}(s)|^2$, where N is the frequency division factor of the PLL. Although the phase noise of the reference is typically lower than that of the VCO by many orders of magnitude, it may become comparable to the VCO noise, if a large division factor is employed. For instance, the value of $N=1024$ in [1] corresponds to an increase of the phase noise by about 60 dB as it appears at the PLL output. The VCO noise spectrum in the PLL is high-pass filtered by the function $|H_{HPF}(s)|^2 = |1 - H_{LPF}(s)|^2$.

In addition to noise filtering due to PLL operation, the removal of the common phase error (CPE) in an OFDM system results in further high-pass filtering [11]. In an OFDM system the carriers are separated by the carrier spacing $(\Delta f)_{car} = 1/T_u$, where T_u is the useful part of the symbol length, that is, the length of the Fourier transformation interval [8]-[10]. Combining all these effects, we obtain for the weighted PLL phase noise spectrum

$$S_{PLL} = \left(S_{VCO} |1 - H_{LPF}|^2 + N^2 S_{REF} |H_{LPF}|^2 \right) \times \left[1 - \text{sinc}^2(f T_u) \right], \quad (4)$$

where the “sinc” function is defined by $\text{sinc}(x) = \sin(\pi x)/(\pi x)$. The rms phase error, sometimes called absolute phase jitter, is given by [7]

$$\sigma_\phi [\text{rad}] = \sqrt{2 \int_0^{B/2} df S_{PLL}(f)}. \quad (5)$$

The upper integration limit is half the bandwidth of the whole OFDM band. This corresponds to the

“middle-carrier” weighting function as representative for the whole OFDM signal [11]. A PLL is usually modeled as a second-order system. For the charge-pump PLL under consideration the LPF transfer function is given by [14]

$$H_{\text{LPF}}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \quad (6)$$

where ζ is the damping factor, and ω_n is the natural angular frequency. For $\zeta > 1$ the PLL can be approximated by a first-order system according to

$$H_{\text{LPF}}(s) \approx \frac{\omega_l}{s + \omega_l}, \quad (7)$$

where the loop bandwidth (in rad/s) is given by $\omega_l = 2\zeta\omega_n$. Equation (5) in conjunction with (4) and the filter function (6) or (7), respectively, allows the effective phase error σ_ϕ to be calculated from circuit parameters and carrier spacing. We will show that σ_ϕ can be used as a figure of merit for the PLL phase noise performance, which allows a fast PLL optimization for a low bit error rate (BER).

IV. NUMERICAL RESULTS

We consider a PLL for 60 GHz described in [1] with a divider ratio of $N = 1024$ and a VCO phase noise of -90 dBc/Hz at 1 MHz offset as reported in [7]. The damping factor $\zeta = 0.5$ represents a typical value for integrated RF synthesizers. We assume a carrier spacing of 1.5625 MHz corresponding to $T_u = 640$ ns. Figure 6 shows the phase error according to (5) as a function of the loop bandwidth $f_L = 2\zeta\omega_n/(2\pi)$ for three different phase noise levels of the reference. As evident, for a low reference noise

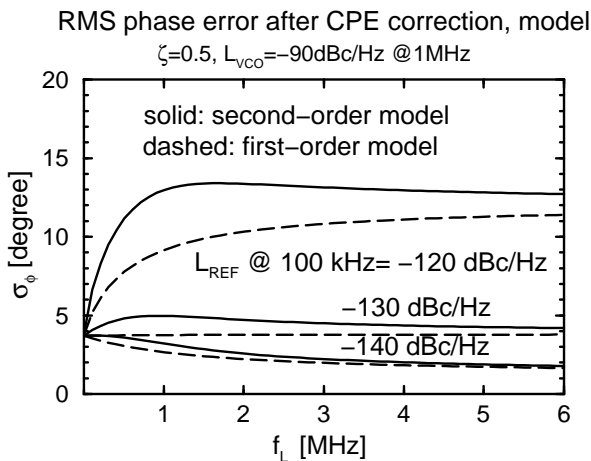


Fig. 6. RMS phase error according to (5) as a function of the PLL bandwidth for three different phase noise levels of the reference oscillator.

level a wideband PLL is useful for a low jitter, while for a high reference noise level a narrowband PLL

is recommended. The jitter predicted by the first-order model is somewhat too optimistic, but gives a rough estimation of the expected phase jitter. Figure 7 shows the rms phase error after CPE correction from time-domain simulation. The close agreement

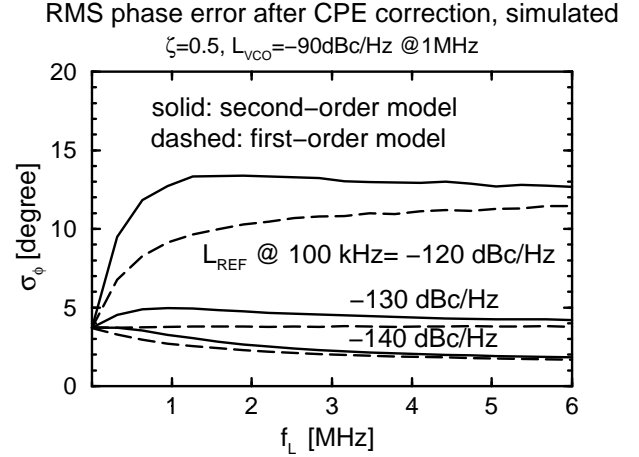


Fig. 7. RMS phase error from time-domain simulation as a function of the PLL bandwidth for the same conditions as Fig. 6.

between Fig. 7 and Fig. 6 demonstrates the high accuracy of both the time-domain simulation and the frequency-domain model.

In order to relate the phase error to the BER of an OFDM system, we have simulated an uncoded 16-QAM system including phase noise in the time domain. The OFDM signal consists of 192 data subcarriers and 16 pilot subcarriers. The latter are used for CPE cancellation in each symbol. All subcarriers are transmitted with the same power. Figure 8 shows the simulated BER for the same conditions as for Fig. 6. Here we assumed identical PLLs for the

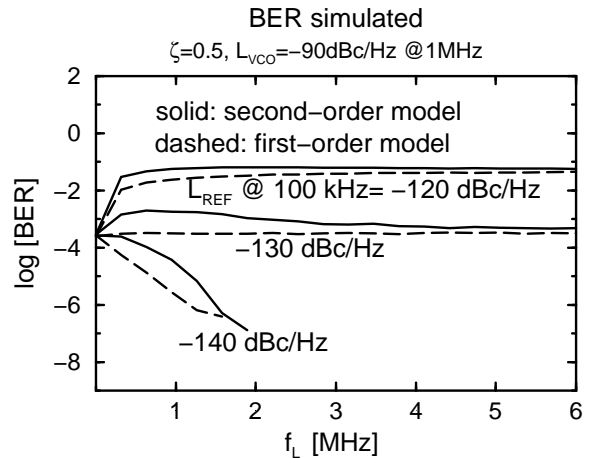


Fig. 8. Simulated bit error rate as a function of the PLL bandwidth for the same conditions as Fig. 6.

transmitter and the receiver with uncorrelated noise.

Obviously, there is a strong correlation between the phase error and the BER. This suggests that (5) is suited for a fast optimization of the PLL loop dynamics of RF synthesizers for OFDM systems.

V. CONCLUSION

We have presented a frequency plan for a 60 GHz OFDM transceiver. The frequency plan with an IF frequency of about 5 GHz facilitates re-use of circuit blocks developed for IEEE 802.11a. A frequency-domain phase noise model for a charge-pump PLL was presented. It includes phase noise of the reference and of the VCO. In addition to noise filtering due to PLL operation, the weighting function concept [11] is applied to incorporate the cancellation of the common phase error. As a result, a simple model for the effective PLL phase jitter is obtained. A 16-QAM OFDM system for the 60 GHz band was simulated in the time domain. It includes phase noise of transmitter and receiver PLL based on measured data. The resulting bit error rates are strongly correlated with the phase jitter σ_ϕ . Therefore, σ_ϕ can be used as a figure of merit for PLL jitter. This allows a fast optimization of PLL parameters. The approach may help to identify, if a certain technology (InP, GaAs, SiGe, CMOS) is suited for a particular modulation scheme (QPSK, 16-QAM, 64-QAM).

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REFERENCES

- [1] W. Winkler, J. Borngräber, B. Heinemann, and F. Herzel, "A Fully Integrated BiCMOS PLL for 60 GHz Wireless Applications," *ISSCC Digest of Technical Papers*, San Francisco, Feb. 2005, pp. 406-407.
- [2] M. Mansuri and C.-K. K. Yang, "Jitter Optimization Based on Phase-Locked Loop Design Parameters," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1375-1382, Nov. 2002.
- [3] A. Mehrotra, "Noise Analysis of Phase-locked Loops," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 49, pp. 1309-1316, Sep. 2002.
- [4] D. C. Lee, "Analysis of jitter in phase-locked loops," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 49, pp. 704-711, Nov. 2002.
- [5] K. Kundert, "Predicting the Phase Noise and Jitter of PLL-Based Frequency Synthesizers," in *Phase-Locking in High-Performance Systems*, Ed. Behzad Razavi, John Wiley & Sons, 2003, pp. 46-69.

- [6] F. Centurelli, A. Ercolani, G. Scotti, P. Tommasino, and A. Trifiletti, "Behavioral Model of a Noisy VCO for Efficient Time-Domain Simulation," *Microwave and Optical Technology Letters*, vol. 40, pp. 352-354, Mar. 2004.
- [7] F. Herzel, W. Winkler and J. Borngräber, "Jitter and Phase Noise in Oscillators and Phase-locked Loops," in *Proc. SPIE Fluctuations and Noise*, Maspalomas, Gran Canaria, Spain, May 2004, vol. 5473, Noise in Communication, pp. 16-26.
- [8] T. Pollet, M. van Bladel, and M. Moeneclaey, "BER sensitivity of OFDM systems to carrier frequency offset and Wiener phase noise," *IEEE Trans. on Communications*, vol. 43, pp. 191-193, Feb. 1995.
- [9] L. Tomba, "On the effect of Wiener phase noise in OFDM systems," *IEEE Trans. on Communications*, vol. 46, pp. 580-583, May 1998.
- [10] A. García Armada, "Understanding the Effects of Phase Noise in Orthogonal Frequency Division Multiplexing (OFDM)," *IEEE Trans. on Broadcasting*, vol. 47, pp. 153-159, June 2001.
- [11] J. Stott, "The effects of phase noise in COFDM," *BBC Research and Development*, EBU Technical Review, Summer 1998.
- [12] W. Rave, D. Petrovic, and G. Fettweis, "Performance Comparison of OFDM Transmission affected by phase noise with and without PLL," in *Proc. International Workshop on Multi-Carrier Spread-Spectrum (MC_SS)*, Oberpfaffenhofen, Germany, Sep. 2003.
- [13] F. Herzel, G. Fischer, and H. Gustat, "An Integrated CMOS RF Synthesizer for 802.11a Wireless LAN," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1767-1770, Oct. 2003.
- [14] B. Razavi, *RF Microelectronics*, Prentice-Hall, Upper Saddle River, 1998.