

A Fully Integrated 60 GHz LNA in SiGe:C BiCMOS Technology

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Abstract — This paper presents a SiGe differential low-noise amplifier (LNA) for the V-band. The measured gain at 60 GHz is 18 dB, and the input return loss is below -15 dB. The 3-dB bandwidth is from 49 GHz to 71 GHz. Measured and simulated S-parameters agree well over the whole range. The LNA draws 30 mA from a 2.2 V supply. It facilitates the design of a fully integrated WLAN receiver in the 57-64 GHz band.

Index Terms — LNA, SiGe:C Bipolar/BiCMOS, Microwave Monolithic Integrated Circuits (MMIC), 60 GHz, Differential Amplifier.

I. INTRODUCTION

The 7 GHz unlicensed band around 60 GHz provides the possibility of gigabit-per-second wireless communication. One promising application is the gigabit WLAN.

Up until now, III/V technologies offer the fastest transistors at good noise performance. However, the possible integration level is moderate and the cost is relatively high. By contrast, silicon-based technologies are cheaper and lend themselves to high integration. Recently, SiGe heterojunction bipolar transistors (HBTs) with an f_T of 375 GHz have been reported [1]. Using SiGe bipolar technology, an integrated LNA and a mixer working at 60 GHz have been demonstrated [2]. SiGe-BiCMOS technologies offer a still higher integration level, since they are compatible with CMOS technology [3]. Using SiGe:C BiCMOS technology, a 60 GHz LNA [4] and a fully integrated RF synthesizer [5] have been presented recently. For very-low-cost transceivers, CMOS is a possible candidate. A first 60 GHz LNA-mixer combination in 0.13 μm CMOS was presented recently showing a combined noise figure of 12.5 dB [6].

This paper presents an LNA in SiGe:C BiCMOS technology combining a high gain with excellent input matching. Unlike the LNA in [2], it employs a differential topology, which is more robust to common-mode noise. Furthermore, a differential design is less susceptible to instabilities due to bond-wire inductances. Different types of inductors are compared with respect to quality factor and chip area.

II. LNA TOPOLOGY AND DESIGN METHODOLOGY

A. LNA Topology

In LNA design, the most important specifications are gain and noise figure. In multi-stage LNAs the first stage is usually matched to 50 Ω , where emphasis is placed on achieving a low noise figure. The later stages are matched to maximum gain. The most common topologies are common-emitter (CE), common-base (CB) and cascode. The transistors used in this design allow a simple matching and a wide frequency band for CE. Each stage gives a gain of about 6 dB. Three stages are used in this LNA design. To make the LNA working robustly to bond-wire inductances, a differential topology is used. In such a design there is no amplified signal current flowing through the bond wires for ground and supply. Furthermore, variations of the on-chip ground potential are less harmful in a differential design. The simplified schematic is shown in Fig. 1. In reality, the inductors are replaced by a more sophisticated network discussed in section III.

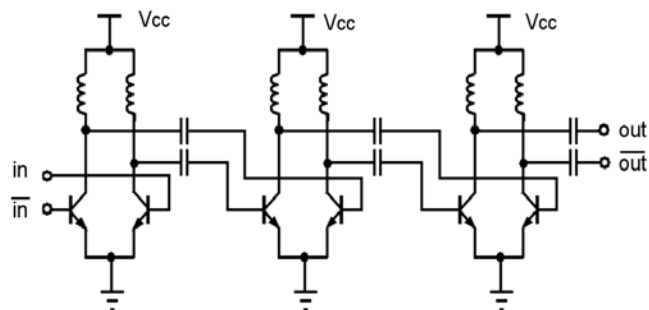


Fig. 1. Simplified schematic of three-stage LNA.

B. Comparison of Three Types of Inductors

In high-frequency circuits, passive devices introduce extra loss and deteriorate the noise performance. The passives include capacitors, resistors and inductors.

Inductors and transmission lines are especially critical, since their Q-factor is rather low due to the lossy substrate and the metal resistance. Furthermore, inductors often occupy most of the chip area in RF circuits. In traditional microwave circuits, the microstrip transmission lines (MTL) are used for matching. With technology scaling, the device and metal size are scaled down deteriorating the Q-factor of the MTL inductors. The other two types of inductors are coplanar waveguide (CPW) inductor and metal line inductor (LI). The latter is realized as a metal strip in the top metal and does not contain a ground plate below. The main advantages and disadvantages are listed below.

- MTL inductors: High-impedance transmission lines are used to build inductors. Due to the narrow width, extra loss is introduced and the Q-factor is low. Transmission lines occupy a large chip area. The coupling between inductors is small facilitating integration.
- CPW inductor: In this type of inductors, both the center conductor and the ground metal are in the top metal layer, which has the lowest resistance. Most of the electromagnetic field concentrates at the slot region minimizing the substrate loss. A degree of freedom is added, since the width of the center conductor and the slot can be changed for a given impedance. This allows a trade-off between resistance and substrate loss. The Q-factor is the highest for CPW. The disadvantage is the use of bridges at discontinuities to remove transmission modes other than TEM mode. The chip area is large due to the ground metal.
- Line inductors: The inductance is the highest for a given chip area. This tends to increase the Q-factor. But, on the other hand, because the electromagnetic field penetrates into the lossy substrate, the Q-factor is reduced. The coupling between inductors is high. So line inductors have to be used with care not to damage the design by inductor coupling.

Figure 2 shows EM simulation results for these three types of inductors. A typical inductance value of 0.1 nH was chosen for these inductors. The EM simulation was verified by measurement of some special structures. The simulation and measurement results match quite well. For calculation of Q-factor and inductance, one end of the inductors is connected to ground. Then impedance, inductance and Q-factor are calculated as follows:

$$Z_{11} = Z_0 \frac{1 + S_{11}}{1 - S_{11}}, \quad (1)$$

$$L = \frac{\text{Im}(Z_{11})}{\omega}, \quad (2)$$

$$Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})}. \quad (3)$$

The inductors have been optimized for a high Q at 60 GHz, where the CPW inductor exhibits a Q as high as 17. The Q-factors of metal line inductor and MTL inductor are 13 and 10, respectively. Metal line inductor has the smallest chip area and a moderate Q-factor, so it was chosen for this LNA design as inductive loads and for input matching. In addition, microstrip transmission lines are used to spatially separate the inductors.

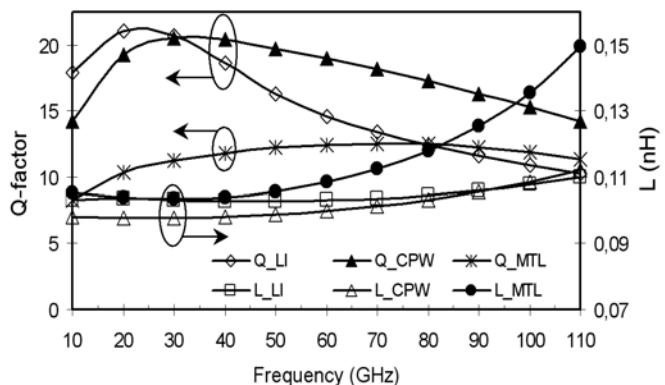


Fig. 2. Q-factors and inductance for the three types of 0.1 nH inductors.

C. Design of Inductors and Transmission Lines

The top metal (metal 4) is used to build the transmission lines, and metal 1 is used to construct the ground plate. Because the silicon dioxide layer is very thin, this transmission line has a loss of 1.3 dB / mm at 60 GHz. In order to build a high-Q inductor, the series resistance has to be low, and the shunt parasitic capacitance has to be small. At high frequencies, the skin effect causes the series resistance to increase. An optimum line width of 6 μm results from this trade-off. The lumped model is constructed by eight components instead of nine components as in [7]. This is because there is no metal overlap in these inductors, so that the series capacitor connecting input to output can be neglected. The model is shown in Fig. 3. The S-parameters are shown in Fig. 4, both for the lumped model and for EM simulations. The transmission line model is built by removing the C_{SI} and R_{SI} in the inductor model, which is also shown in Fig. 3. The silicon effect, modeled by C_{SI} and R_{SI} , is eliminated by the transmission line ground metal. We disregarded the frequency dependence of the skin effect in the lumped model, and fitted the series resistance at 60 GHz.

D. RF Pads

The RF pads are constructed by using a ground plate below the pads to isolate the silicon substrate from the pads. These pads can be modeled by a single capacitor. In our LNA design, these pad capacitors are involved in the matching of the input and output of the LNA to $50\ \Omega$. The capacitance can be calculated by using metal-insulator-metal capacitor equation. An extra 15 percent due to the edge effect is added to the total capacitance.

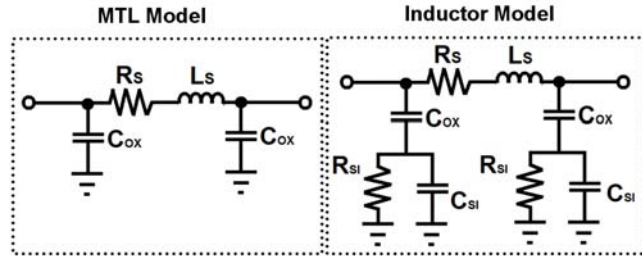


Fig. 3. Transmission line and inductor model.

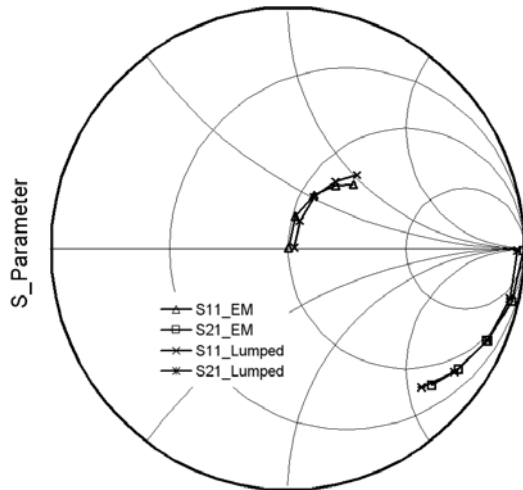


Fig. 4. Simulated S-parameters from 1 GHz to 110 GHz for lumped inductor model and EM simulations.

III. DESIGN OF THE LNA

The bipolar transistors used in the LNA have an f_T of 180 GHz and an f_{max} of 200 GHz. The input matching topology is shown in Fig. 5. The capacitor C_1 is used to bypass high frequencies to ground. Capacitor C_2 is a DC-block capacitor. C_3 models the pad capacitance, which is used together with two transmission lines to match the LNA input. DC current flows into the circuit from V_B through an inductor and a transmission line to the transistor base. The transmission lines are used to separate

the inductor from the inductive load of the first stage and the input pad to reduce magnetic coupling. The output matching circuit is shown in Fig. 6. The capacitor C_1 is used to bypass high frequencies to ground. A resistor is used to lower the gain at low frequencies. The transmission line is used to separate the load inductor L_C from the output bond pad. C_3 models the bond-pad capacitance, and C_2 is a DC blocker. For the inter-stage matching, the transmission line and bond-pad capacitor are removed in the output matching circuit. The DC bias circuitry is also shown in Fig. 6. The LNA was designed to match the input close to the minimum noise figure. The collector currents increase gradually from the first stage to the third stage to increase the gain while keeping the noise figure small. Each stage is designed to be unconditionally stable. By doing so, the LNA becomes unconditionally stable as well.

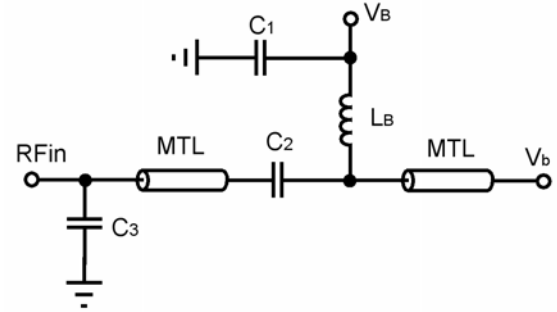


Fig. 5. Input matching circuit.

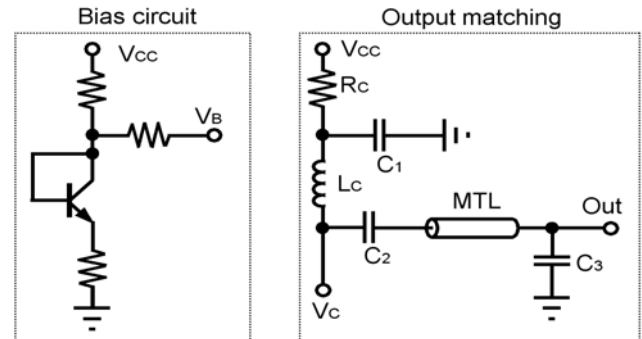


Fig. 6. Bias circuit and output matching.

The LNA is supposed to work differentially. But the measurement of a differential circuit turns out to be difficult at such high frequencies. The first idea to solve the measurement problem would be to design an on-chip balun [4]. Such a balun introduces loss and increases the noise figure. However, there is another simple way to solve the measurement problem. The emitters are connected directly to ground as shown in Fig. 1, so that each path can be measured separately as a single-ended LNA.

IV. MEASUREMENT RESULTS

The final LNA layout occupies a chip area of 0.6 mm x 0.7 mm. It comprises eight inductors and nine transistors. All matching and bias circuits are integrated. The measurement and simulation result are shown in Fig. 7. Figure 8 shows a chip photograph of the LNA. The measured gain is about 18 dB at 60 GHz. The 3dB-bandwidth amounts to 22 GHz ranging from 49 GHz to 71 GHz. The input return loss is lower than -15 dB within this range, and the output return loss is lower than -7 dB. From DC up to 110 GHz, the LNA is unconditionally stable. The measurement results and the simulation results match very well at the center frequency of 60 GHz. There are only small deviations below and above, which are partly due to inaccuracies of the passive lumped models. Unfortunately, the noise figure could not be measured due to the lack of measurement equipment. The simulated noise figure NF50 amounts to 6.8 dB at 60 GHz. Due to good matching, NF50 equals the simulated minimum noise figure NFmin. The LNA is robust to DC voltage variations. With the DC voltage varying from 1.6 to 2.8 V, the performance changes only slightly. The gain variation is as low as 1 dB. The LNA draws 30 mA from a 2.2 V supply.

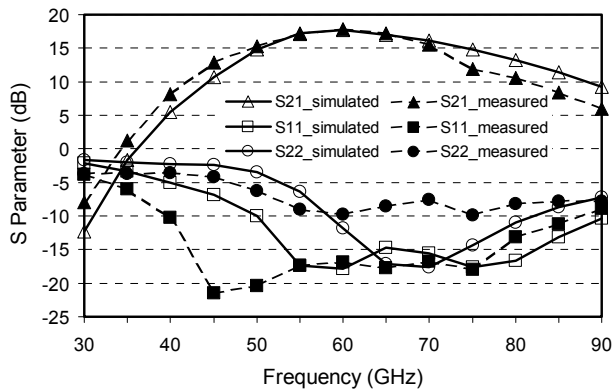


Fig. 7. Measured and simulated S-parameters.

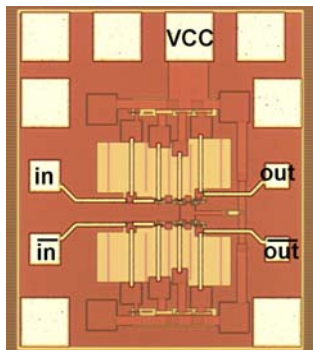


Fig. 8. Chip photo of the LNA.

V. CONCLUSION

A three-stage differential LNA for the V-band has been presented. It has a 3 dB-bandwidth of 22 GHz, which ranges from 49 GHz to 71 GHz. It comprises the relevant frequency band from 57 GHz to 64 GHz plus some safety margin to compensate for the variations of device parameters with process and temperature. A gain of 18 dB was measured at 60 GHz. The input return loss is as low as -15 dB and the output return loss is better than -7 dB over the whole 3 dB-bandwidth.

All matching structures and the bias circuitry have been integrated on chip. A 0.25 μm SiGe-BiCMOS technology was used to fabricate the LNA. Three types of inductors have been compared with respect to chip area and Q-factor. All inductors and transmission lines have been modeled by lumped elements. The models have been verified by EM simulation and measurement. Bond-pads with a bottom ground layer are used in this LNA to minimize signal coupling to ground. This LNA is especially suited for 60 GHz wireless local area network (WLAN) working at very high data rates.

ACKNOWLEDGEMENT

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