

High-Frequency Low-Noise Amplifiers and Low-Jitter Oscillators in SiGe:C BiCMOS Technology

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ABSTRACT

This paper describes the design of noise-critical circuits for radio-frequency and high-speed digital applications in a SiGe:C BiCMOS technology. Starting with a figure of merit for the high-frequency noise behavior of bipolar transistors, challenges in the transistor design are formulated. It is shown that the addition of carbon to the base of a SiGe-HBT results in an excellent high-frequency noise behavior of the transistors. A first design of a differential three-stage low-noise amplifier for 60 GHz applications is presented having a gain of 18 dB at 50 GHz. Furthermore, a 60 GHz voltage-controlled oscillator is presented with a phase noise of -90 dBc/Hz at 1 MHz offset from the oscillation frequency. Using a first-order PLL model, we predict an rms jitter contribution to a 5 MHz-bandwidth PLL as low as 0.4 percent of the oscillation period. Possible applications include wireless and wired broadband communication as well as automotive radar.

Keywords: High-frequency noise, SiGe-HBT, SiGe:C, BiCMOS, low-noise amplifier, low-jitter oscillator

1. INTRODUCTION

The growing market in wireless and fiber-optic communication requires transistors working at tens of GHz. Examples are wireless LAN in the 60 GHz ISM band and 40 Gb/s fiber-optic networks. In order to obtain a high sensitivity in receivers for such networks, the front-end circuits must have a low noise. Due to the universal power-noise tradeoff, a low noise directly translates into a low power consumption, which is crucial for battery-driven devices. Another growing field for low-noise transistors are fiber-optic receivers working at data rates of 40 Gb/s and higher, where the jitter requirements for the clock and data recovery are difficult to meet. This is especially true for integrated low-cost implementations, where the low quality factor of integrated passives and the feedback through the bond connections make the design of stable low-noise circuits a challenging task.

Systems on a chip (SoC) require RF circuitry to be integrated together with digital circuitry working at a lower speed. For the latter, CMOS is the best choice due to the low power consumption at low and moderate clock rates. A perfect technology would combine bipolar transistors for the RF part and CMOS for the low-speed part of the system. BiCMOS technology combines the advantages of high-speed bipolar and CMOS. This combination is useful not only for SoC, but also for circuits with a moderate integration level. An example is a radio frequency synthesizer, where a high-frequency voltage-controlled oscillator (VCO) followed by a high-speed frequency divider needs to be combined with programmable low-speed counters for controlling the output channel²². At frequencies of 60 GHz the availability of low-noise HBTs will enable the integration of a complete frequency synthesizer, which is underway. But also at lower frequencies, where CMOS can be used for SoC designs, one can benefit from low-noise HBTs, since some bipolar circuits such as frequency dividers consume much less power than their CMOS counterparts. Another important field of SiGe-HBT applications are high-speed optical communication circuits⁷. Greater levels of integration on a single chip will provide higher performance and lower cost. As a result, SiGe BiCMOS technology will continue to take over territories thus far claimed by GaAs and InP technologies.

This paper describes low-noise transistors, a low-noise amplifier for 60 GHz, and a 60 GHz voltage-controlled oscillator fabricated in a SiGe:C BiCMOS technology. The measured noise parameters are promising for RF and radar applications.

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2. DESIGN CONSIDERATIONS FOR LOW-NOISE TRANSISTORS

The high-frequency device noise in the GHz range is dominated by white noise (shot / thermal). By contrast, flicker noise is not relevant for *linear* radio frequency (RF) circuits such as low-noise amplifiers (LNA), since the power spectral density (PSD) of flicker noise is very small at RF. The effect of flicker noise in nonlinear circuits such as oscillators will be briefly discussed in section 4. The noise figure (NF) of bipolar devices is flat in the upper MHz range and starts to increase with frequency somewhere in the lower GHz range, depending on the technology. While the plateau value of the NF is mainly determined by the static current gain β_0 , the frequency where the NF starts to increase is determined by other device parameters. To illustrate this point, we look at a simple figure of merit (FOM) describing the high-frequency noise of a (hetero-) bipolar transistor. Based on a work of de Graaff et al.¹, Baltus² has defined a frequency $f_{0.5}$, where the noise NF at optimum current has increased by 0.5dB compared to the plateau value. It is given by

$$f_{0.5} = 0.1 \sqrt{\frac{f_T}{4\pi R_b (C_{jc} + C_{je})}}. \quad (1)$$

This equation illustrates the requirements to the device parameters of low-noise transistors, which are: (1) a low base resistance R_b , (2) a low collector junction capacitance C_{jc} , (3) a low emitter junction capacitance C_{je} , and (4) a sufficiently high a.c. current gain roughly given by f_T / f , where f_T is the transit frequency and f the radio frequency of interest. The optimisation of these parameters entails several tradeoffs. First, a low doping level of the low-doped collector (LDC) will decrease C_{jc} , but also f_T . Second, a thinner base at a given boron concentration will improve f_T , but increase the base resistance. Third, a relatively thick low-doped emitter layer (LDE) will lower C_{je} , but reduce f_T . The final vertical profile was optimized by using 2D device simulation.³ The result of such an optimization is schematically shown in Figure 1. The profile enables a maximum transit frequency f_T and maximum oscillation frequency f_{max} of 200 GHz each.⁴

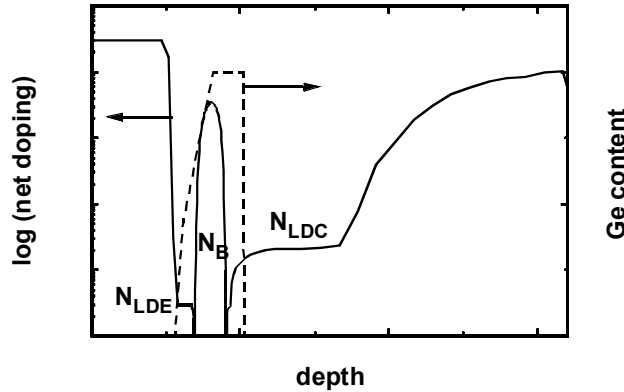


Figure 1. Doping concentration and Germanium content versus depth (not to scale).

Note that the half-graded Ge profile is flat over the collector side of the base, but graded over the emitter side of the base. In this region, the electrical counter-field produced by the boron grading is overcompensated by the Ge grading to minimize the base transit time.

A critical point in the fabrication of SiGe-HBTs is the boron diffusion during the annealing steps following the deposition of boron in the base. With increasing boron diffusion, the base width will increase and the transit frequency will degrade. Furthermore, a strong boron diffusion limits the allowable boron dose, since boron out-diffusion out of the SiGe layer must be prevented in any case. A relatively small amount of carbon in the SiGe layer is well-suited to minimize the boron diffusion⁶. It allows a large boron dose to be deposited resulting in a low base resistance while keeping the base width small, which results in a small transit time.

Figure 2 shows the measured minimum noise figure NF_{min} of an HBT in our SGC25C SiGe:C BiCMOS technology⁴ as a function of frequency. In addition, the noise figure with a 50 Ω source impedance (NF_{50}) is also plotted. While at low

frequencies NF50 is much larger than NFmin, the difference becomes smaller at higher frequencies. This indicates that impedance matching to 50 Ω maintaining a good noise performance should be possible at frequencies of 30 GHz and above. The associated gain is shown in Figure 3. Obviously, a high current density improves the gain, but deteriorates the noise figure. Nonetheless, a high collector current may be necessary at the expense of a higher noise figure in order to achieve the required gain at very high frequencies.

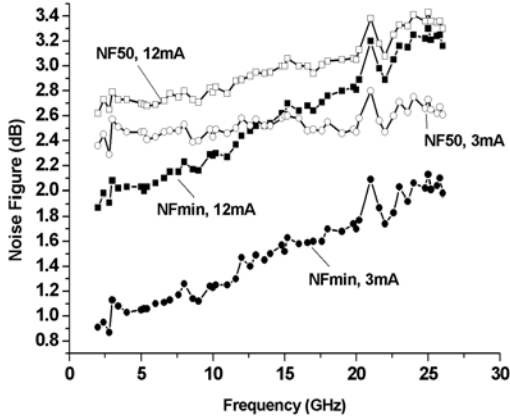


Figure 2. Minimum noise figure and 50 Ω noise figure as a function of frequency for two collector currents.

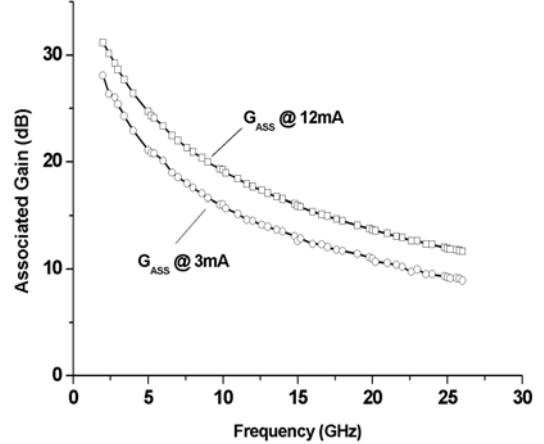


Figure 3. Associated gain as a function of frequency for two different collector currents.

The effective emitter size is $2.3 \mu\text{m}^2$, which is close to the optimum for 60 GHz. For applications at lower frequencies the transistor size should be increased in proportion to the inverse frequency to facilitate matching.

3. LOW-NOISE AMPLIFIERS

3.1. Noise parameters for circuits and transistors

A low-noise amplifier (LNA) has to amplify a weak signal that is superposed by noise at the same frequency. The noise will be amplified by the same factor as the signal. Therefore, the signal-to-noise ratio (SNR) at the output cannot be larger than at the input. In reality, the transistors and resistors in the amplifier contribute noise that makes the SNR at the output smaller than at the input. The noise factor of a linear two-port (or four-pole) is defined as the SNR ratio between input and output according to

$$F = \frac{(SNR)_{in}}{(SNR)_{out}} > 1. \quad (2)$$

It quantifies the degradation of the SNR by noise sources in the amplifier. When expressed in decibel (dB), this expression is called noise figure

$$NF = 10 \log_{10}(F) > 0 \text{ dB}. \quad (3)$$

The noise figure strongly depends on the source impedance Z_S that drives the circuit. In the case of an LNA, the circuit is driven by a 50 Ω antenna. In LNA noise figure measurements, the antenna is replaced with a signal generator the output impedance of which is also 50 Ω. The 50 Ω noise figure is the noise figure with this input termination

$$NF_{50} = NF |_{Z_S=50\Omega} \quad (4)$$

NF₅₀ is the most important figure of merit for LNAs. The first stage of an LNA is typically a bipolar transistor in common-emitter configuration. The antenna is usually not directly connected to the base of this transistor. Instead, a passive network is placed between the antenna and the base to transform the 50 Ω impedance of the antenna to a desired value. Therefore, the generator admittance driving the transistor can be chosen arbitrarily (ideally). The value of Z_S where the noise figure is a minimum is called optimum input impedance Z_{opt} . The corresponding noise figure is called minimum noise figure

$$NF \min = NF |_{Z_S = Z_{opt}} \quad (5)$$

This is the most relevant figure of merit for low-noise *transistors*. Obviously, NF₅₀ cannot be lower than NF_{min}. If NF₅₀ is close to NF_{min}, then the optimum source impedance is close to 50 Ω. This is especially desirable if the base of the transistor is connected to a 50 Ω antenna, since input matching at low noise is facilitated.

3.2. LNA Measurements

To demonstrate the suitability of SiGe:C technology for millimeter wave applications we have designed an experimental 60 GHz LNA. In the literature no silicon-based amplifiers have been presented for this high frequency range thus far. Gramegna et al. presented an 8.2 GHz LNA and gave an overview of recent LNA implementations in SiGe technologies for 0.9 to 23 GHz.⁹

To obtain sufficient gain, a three-stage implementation was chosen. Figure 4 shows the basic circuit of one stage of the LNA. The fully differential approach has two advantages. First, the differential topology exhibits a better immunity to bond wire and other parasitic interconnect inductors, since ideally no signal current flows through them. This results in a higher gain and reduced tendency to unwanted oscillations. The second advantage is its lower sensitivity to noise in the supply and substrate voltages. This is especially advantageous in a highly integrated environment feasible in a SiGe:C BiCMOS technology.

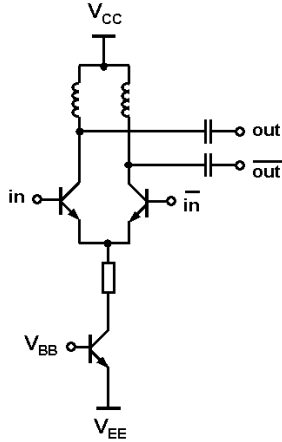


Figure 4. Implementation of one LNA stage.

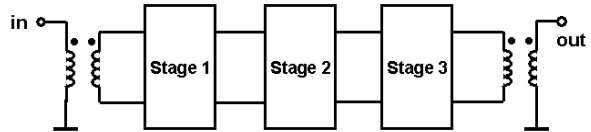


Figure 5. Differential 3-stage LNA.

Figure 5 shows the entire schematic of the 60 GHz LNA. It consists of three identical stages according to Figure 4. Two integrated transformers at input and output convert the single-ended signal coming from the antenna to the internal differential signal and, conversely, back to the single-ended path required in the measurement set-up at the LNA output. Between the amplifier stages matching networks for optimum power transfer are inserted. The LNA characteristics were measured on-wafer with an Agilent network analyzer 8510XF. Figure 6 shows the gain parameters of the LNA in the frequency range from 2.4 GHz to 110 GHz. The measured and the simulated transmission power gain are in a good correspondence in the frequency range between 20 GHz and 50 GHz. The goal of 15 dB power gain at 60 GHz was not met in the first design cycle of the LNA.

We have measured the noise parameters of the LNA with an ATN noise system in a 2–26 GHz frequency band. Figure 7 shows the measurement results. We observe NF₅₀ approaching NF_{min} in the upper frequency range of the noise measurement system. At 26 GHz NF_{min} is 6 dB and NF₅₀ is 6.5 dB.

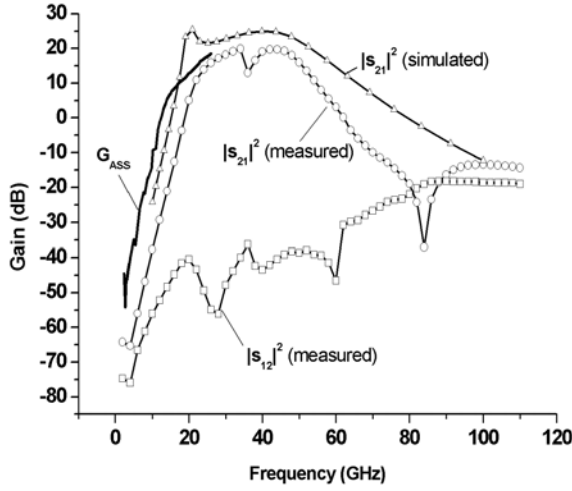


Figure 6. Measured associated gain and transmission power gain of the LNA as a function of frequency.

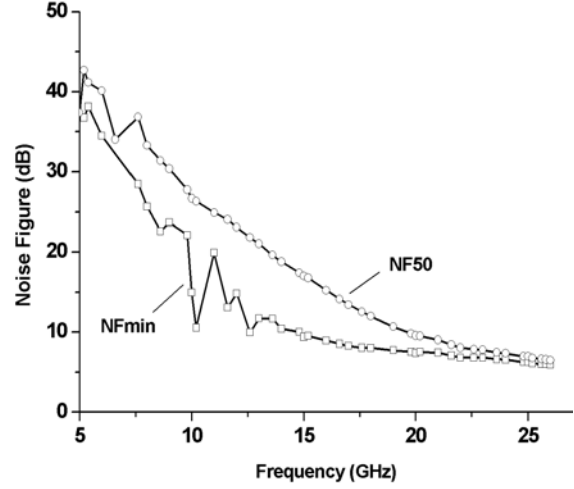


Figure 7. Minimum noise figure and 50 Ω noise figure as a function of frequency.

4. LOW-JITTER OSCILLATORS

4.1. Phase noise and jitter

Voltage-controlled oscillators (VCO) are critical building blocks in integrated fiber-optic receivers, since they must have a low jitter. High quality factors of the resonance circuits are needed to meet the stringent jitter requirements imposed on clock and data recovery (CDR) circuits working at data rates of 40Gb/s and higher. Low-jitter VCOs are also required for radio-frequency (RF) synthesizers. Low-cost realizations of CDR circuits and RF synthesizers require the VCO to be integrated on a silicon chip. The VCO may become the dominant source of jitter in such applications⁷ due to the low quality factors of integrated inductors and capacitors. In the last decade many publications on phase noise⁸⁻¹³ and jitter¹⁴⁻¹⁷ in oscillators have been published. Also, increasing effort has been devoted recently to describing jitter in phase-locked loops (PLL)¹⁸⁻²³.

Flicker noise is small at RF, but in non-linear circuits such as oscillators it can be converted to RF by unwanted mixing processes to frequencies around the signal. In most cases, however, the resulting up-converted noise can be eliminated by using feedback in the form of phase-locked loops (PLL). In most high-speed digital PLLs the loop bandwidth is as large as a few MHz and, thus, much larger than the $1/f$ noise corner frequency of the transistor. Since the VCO noise is high-pass filtered in a PLL, flicker noise will be sufficiently suppressed in these applications.

In theory, the power spectral density (PSD) of the phase is often used to describe phase noise. This quantity, however, is hard to measure. Another type of phase noise is the relative single-sideband phase noise, which is defined as the *one-sided* PSD of the output voltage normalized to the power in the fundamental tone $V_0^2/2$. According to the Wiener-Khinchine theorem it is related to the auto-correlation function (ACF) according to

$$S_{SSB}(\omega) = \frac{4}{V_0^2} \int_{-\infty}^{\infty} d\tau \langle V(\tau)V(0) \rangle \exp(-j\omega\tau), \quad (6)$$

where the brackets denote the ensemble average. When expressed in dBc/Hz, this quantity is denoted as \mathcal{L} and defined by

$$\mathcal{L}[\text{dBc/Hz}] = 10 \log_{10} (S_{SSB}(\omega)[1/\text{Hz}]). \quad (7)$$

The quantity \mathcal{E} is usually displayed by commercial phase noise meters.

The time between the n^{th} and $(n+1)^{\text{th}}$ minus-to-plus zero crossing of the oscillator output $V(t)$ is referred to as T_n . In an ideal oscillator T_n is independent of n and equals the average period $T=1/f_0$. In reality, T_n depends on n due to noise in the circuit. The absolute jitter ΔT_{abs} is the deviation of the zero crossing from the ideal position, that is,

$$\Delta T_{\text{abs}}(n) = \sum_{i=1}^n (T_i - T) . \quad (8)$$

The absolute PLL jitter can be measured by using an oscilloscope. It results from the noise of the reference (typically a crystal oscillator) and the noise of the VCO locked to this reference. For integrated PLLs noise of the reference can usually be neglected, since the VCO noise has a much stronger impact on the PLL jitter²⁰. The phase noise of the VCO is high-pass filtered when placed in a PLL. With this assumption and assuming a first-order PLL of loop bandwidth f_L [Hz], the standard deviation of the absolute PLL jitter in the steady state can be expressed in terms of f_L and the phase noise of the free-running VCO²³

$$\sigma_{\text{abs}}^{\text{PLL}} = \frac{\Delta f}{f_0} \sqrt{\frac{S_{\text{SSB}}^{\text{VCO}}}{4\pi f_L}} . \quad (9)$$

It is important to note that the single-sideband phase noise must be taken at an offset Δf from the carrier f_0 in the region of the spectrum with a -20dB/decade slope, where S is proportional to $1/(\Delta f)^2$. Equation (9) allows the PLL jitter due to VCO noise to be calculated from the phase noise of the free-running VCO, which is typically known before the final PLL design. This may save design cycles and, thereby, cost.

In a second-order PLL model the high-pass filter of the second-order PLL takes the form²⁴

$$\left| \varphi_{\text{out}} / \varphi_{\text{VCO}} \right|^2 = \left| \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right|^2 , \quad (10)$$

where $s = j\omega = j2\pi\Delta f$, ζ is the damping factor and $\omega_n = 2\pi f_n$ the natural angular frequency. For the second-order PLL model we obtain

$$\sigma_{\text{abs}}^{\text{PLL}} = \frac{\Delta f}{f_0} \sqrt{\frac{S_{\text{SSB}}^{\text{VCO}}}{8\pi\zeta f_n}} . \quad (11)$$

4.2. VCO Measurements

We have measured the phase noise of a 60 GHz VCO fabricated in a 0.25 μm SiGe:C BiCMOS technology⁵. Figure 8 shows a chip photograph of the oscillator circuit.

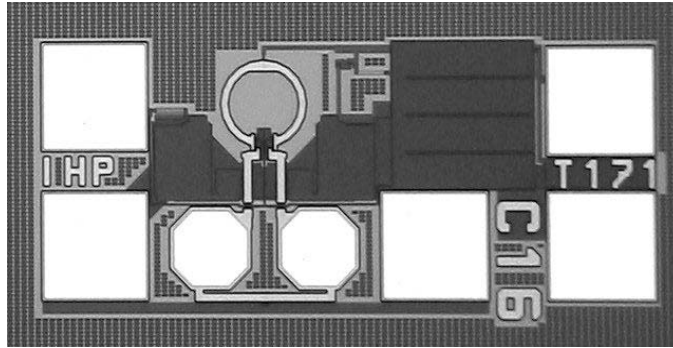


Figure 8 . Photograph of the oscillator chip measuring 0.63 x 0.35 mm².

The tuning range of the VCO is shown in Figure 9. Details about the circuit design of the VCO are described elsewhere²⁵. The VCO was designed as a stand-alone circuit and the phase noise measurement was performed on wafer. The jitter contribution of the VCO in a PLL cannot be measured, since the PLL has not yet been fabricated. Furthermore, jitter measurements are difficult at such high frequencies. In order to get an idea of the jitter performance of a PLL using this VCO, we will apply (9) to the measured VCO phase noise.

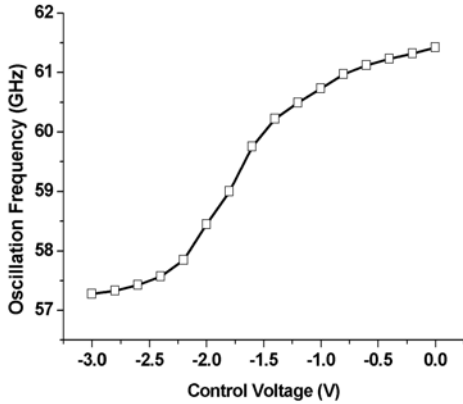


Figure 9. Oscillation frequency as a function of the control voltage.

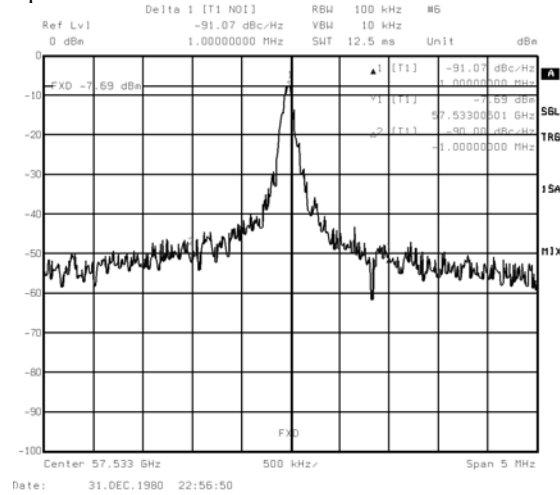


Figure 10. Measured single-sideband phase noise of the free-running oscillator.

Figure 10 shows the phase noise spectrum of the VCO. At a frequency offset of 1 MHz we measured a phase noise of $\mathcal{L} = -90\text{dBc/Hz}$. From (9) we obtain a predicted PLL jitter contribution of 70 fs due to VCO device noise, where a PLL bandwidth of 5 MHz was assumed. This rms jitter corresponds to 0.4 percent of the oscillation period.

5. CONCLUSIONS

We have presented noise measurements on an HBT, an LNA, and a VCO fabricated in the IHP SiGe:C BiCMOS technology. Depending on the collector current, the transistor's minimum noise figure is between 2.0 and 3.2 dB at 26 GHz with an associated gain between 8.8 dB and 11.6 dB. A fully integrated differential LNA shows a measured transmission gain of 18 dB at 50 GHz. The rms jitter contribution of the 60 GHz VCO to a 5 MHz-bandwidth PLL was deduced from phase noise measurements and is as low as 0.4 percent of the oscillation period. Further redesigns will make the circuits suited for 60 GHz WLAN and 77 GHz automotive radar applications.

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